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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

98202702.1

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Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

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Koninklijke Philips Electronics N.V.
5621 BA Eindhoven
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Displaying video on a plasma display panel

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Displaying video on a plasma display panel.

The invention relates to a method of displaying a video signal on a plasma display panel as defined in the precharacterizing part of claim 1. The invention further relates to a circuit for displaying a video signal on a plasma display panel as defined in the precharacterizing part of claim 4. The invention also relates to a plasma display device comprising a plasma display panel and a circuit for displaying a video signal on the plasma display panel as defined in the precharacterizing part of claim 5.

In a known Alternate Lighting In Surface Plasma Display Panel (further referred to as ALIS PDP) with n display lines, each of the display lines comprises a plasma channel to which two spaced apart select electrodes are aligned. Two consecutive plasma channels have one select electrode in common. The display lines are selected in an interlaced sequence to be able to select all display lines of this ALIS PDP one by one. First, during a first display field of display lines, the n/2 odd display lines are selected one by one, then, during a second display field of display lines, the n/2 even lines are selected one by one.

An interlaced video signal has a frame period with a first and a second video field period. Usually, the odd lines of the video signal form the first video field, and the even lines of the video signal form the second video field. When this interlaced video signal has to be displayed on the ALIS PDP, the odd lines of the video signal are displayed on the odd display lines, and the even lines of the video signal are displayed on the even display lines.

When a progressive video signal has to be displayed on the ALIS PDP, two approaches are know dependent on the number of video lines to be displayed. When the number of video lines to be displayed is substantially equal to the number of display lines, the odd lines of the video signal are displayed on the odd display lines. Thus, the even lines of the video signal are not used, and the odd display lines are selected also in periods during which otherwise the even display lines would be selected. When the number of video lines is substantially equal to the half the number of display lines, all the lines of the video signal are displayed on the odd display lines only.

In the situation that interlaced video (for example HDTV) as well as progressive video (for example SXGA) has been displayed on the ALIS PDP, the display of the interlaced video becomes different for the odd and the even display lines.

It is, inter alia, an object of the invention to reduce the differences in the display of the odd and the even display lines.

To this end, a first aspect of the invention provides a method of displaying a video signal on a plasma display panel as claimed in claim 1. A second aspect of the invention provides a circuit for displaying a video signal on a plasma display panel as claimed in claim 4. A third aspect of the invention provides a plasma display with a circuit for displaying a video signal on the plasma display panel as claimed in claim 5. Advantageous embodiments are defined in the dependent claims.

The invention is based on the insight that the display of progressive video on the odd display lines only, as performed in the prior-art, causes the phosphors of the odd display lines to age faster than the phosphors of the even display lines. According to the invention, the progressive video is alternatively displayed on the odd display lines only, or on the even display lines only. In both situations, during a certain period of time which is larger than a field period of the video signal. For example, the period of time is one hour. In this way, the phosphors of the odd and even display lines will age substantially equally and the artifacts during display of the interlaced video signal on all display lines decrease.

In an embodiment of the invention as claimed in claim 2, the number of video lines is smaller than or substantially equal to half the number of display lines. In this way only a few or no video lines will not be displayed on the display lines.

In an embodiment of the invention as claimed in claim 3, the period of time during which the video signal is displayed on the odd or even lines only, is sufficient large to prevent line flicker.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

In the drawings:

Fig. 1 shows part of the structure of a known progressive scanned PDP,

Fig. 2 shows part of the structure of the known ALIS PDP,

Fig. 3 shows a block diagram of a circuit for displaying a video signal on the known ALIS PDP, and

Figs. 4 show voltages supplied to the select electrodes of the ALIS PDP to obtain an interlaced scan.

Fig. 1 shows part of the structure of a known progressive scanned PDP with n display lines D1,..., Dn. Each of the display lines Di comprises a plasma channel Pi to which two spaced apart select electrodes Si1, Si2 are aligned. A display line Di is selected to prime associated pixels Cij (see Fig. 3) by supplying a sufficient high voltage between the two electrodes Si1, Si2. A line of black matrix material Bm separates two consecutive plasma channels Pi, Pi+1.

Because two select electrodes Si1, Si2 are associated with one plasma channel Pi only, it is possible to activate neighboring plasma channels Pi independently. This enables a progressive scan of the plasma channels Pi whereby the plasma channels Pi are activated successively one by one. Detailed information on such a PDP panel and the driving thereof can be found in EP-B-0549275, which is hereby incorporated by reference.

Fig. 2 shows part of the structure of the known ALIS PDP. In the ALIS PDP with n display lines D1,..., Dn, each of the display lines Di comprises a plasma channel Pi to which two spaced apart select electrodes Si, Si+1 are associated. Again, a display line Di is selected by supplying a sufficient high voltage between the two electrodes Si, Si+1. Two consecutive plasma channels Pi, Pi+1have one electrode Si+1 in common. The display lines Di are selected in an interlaced sequence to enable a one by one selection of all display lines Di of this ALIS PDP. First, during a first field of display lines Di, the n/2 odd display lines Di are selected one by one, then, during a second field of display lines Di, the n/2 even display lines Di are selected one by one.

The addressing of the ALIS PDP is elucidated with respect to Fig. 3 and Figs. 4.

Fig. 3 shows a block diagram of a circuit for displaying a video signal Vs on the known ALIS PDP 1. The shown ALIS PDP 1 comprises plasma channels Pi extending in the horizontal direction. Two select electrodes Si, Si+1 are associated with each plasma channel Pi. Data electrodes Daj extend in vertical direction. Overlapping regions of the plasma channels Pi and the data electrodes Daj form display cells or pixels Cij of which one is indicated with a circle.

It is known to generate the gray scales of the displayed video by driving the PDP in a sub-field mode. During each display field a number of sub-fields is generated, each sub-field comprises a prime period and a sustain period. During the prime period, a select driver 2 selects the display lines (rows) Di one by one to prime the display cells Cij of the selected row Di with data signals Dsj. A data driver 3 that receives the video signal Vs supplies the data signals Dsj in parallel. During the sustain period, the select driver 2 supplies pulses to all the rows Di associated with the active display field. The plasma channels Pi are ignited a predetermined times to generate light from the pixels Cij primed to do so. The amount of light produced depends on the number of ignitions. Sustain periods with a different number of ignitions are associated to the different sub-fields in a display field period. The amount of light generated during a display field is the sum of the different amounts of light produced during the sub-fields of this display field. The PDP is able to produce grayscales because during the priming period of each sub-field it is possible to select whether a certain pixel has to produce light during the subsequent sustain period or not. Each sub-field may comprise an erase period, or the erase period may occur once in a display field. During the erase period, all pixels associated with the display field are erased. Detailed information on the sub-field operation of a PDP can be found in EP-B-0549275.

The timing circuit 4 receives the horizontal and vertical synchronization signals S of the video signal Vs to produce the timing signals for the select driver 2 and the data driver 3.

When a progressive video signal Vs has to be displayed on the ALIS PDP, two approaches are know dependent on the number of video lines to be displayed. When the number of video lines to be displayed is substantially equal to the number of display lines Di, only the odd lines of the video signal Vs are displayed on only the odd display lines Di. Thus, the even lines of the video signal Vs are not displayed, and the odd display lines Di are selected also in periods during which otherwise the even display lines Di would be selected.

When the number of video lines is substantially equal to the half the number of display lines Di, all the lines of the video signal Vs are displayed on the odd display lines Di only. The timing circuit 4 commands the select driver 2 to only select the lines of the odd field of display lines Di. The timing circuit 4 may receive information indicating the display mode, or the timing circuit 4 may detect the type of video signal Vs by evaluating the horizontal and vertical synchronization signal of the video signal Vs.

According to the invention, the progressive video Vs is displayed alternatively on the odd display lines Di only, or on the even display lines Di only. In both situations, during a certain period of time which is larger than a field period of the video signal Vs. For example, the certain period of time is one hour, or the certain period of time is related to the time that the display is active. When the display is switched on to normal operation after it had been switched off or entered a standby mode, the video signal Vs is displayed on the other field of display lines Di. The timing circuit 4 may comprise a timer or a memory device, respectively, to generate the certain period in time. The timing circuit 4 commands the select driver 2 to only select the display lines Di of the odd field of display lines, or to only select the display lines Di of the even field of display lines.

Figs. 4 show voltages supplied to the select electrodes Si of the ALIS PDP to obtain an interlaced scan. In all Figs. 4, voltages are denoted with a number 0, 1, -1, -2 to indicate the polarity and the relative value of the voltage concerned. For the sake of simplicity an ALIS PDP with only a few select electrodes Si (S1 to S12), data electrodes Daj (Da1 to Da6) and display lines D1,...,D11 is shown. The voltages supplied to the odd select electrodes S1, S3, ..., S11 are shown to the left of the PDP. The even select electrodes S2, S4, ..., S12 are interconnected in two groups, the voltages supplies to these groups are shown to the right of the PDP. The data voltages Dsj are shown below the PDP. In a selected display line Di, Pixels Cij which are primed to generate light are indicated with a solid circle, pixels Cij which are primed to not produce light are indicated by a dashed circle.

Fig. 4A shows the voltages to select display line D4 during a certain display field. Fig. 4B shows the voltages to select display line D6 during the same display field. Fig. 4C shows the voltages to select display line D5 during a succeeding display field, and Fig. 4D shows the voltages to select display line D7 during this succeeding field.

It is possible to select the display lines Di of a certain display field in different ways. As an example, this is explained with respect to Figs. 4A and 4B. All even rows D2, D4,...,D10 may be selected one by one by first selecting a certain row, let us assume D4, in accordance with Fig. 4A. Next, the consecutive even row D6 is selected as shown in Fig. 4B. Than, the even row D8 is selected in accordance with Fig. 4A by applying a –1 voltage to select electrode S5 and a –2 voltage to select electrode S9. Next, the even row D10 is selected in accordance with Fig. 4B by applying a –1 voltage to select electrode S7 and a –2 voltage to the select electrode S11. And so on. This selecting scheme has the disadvantage that the voltages on the even select electrodes have to change for every display line Di, this causes a large dissipation. This drawback is prevented by first selecting the rows D4, D8 in accordance with Fig. 4A and next the rows D2, D6, D10 in accordance with Fig. 4B. In the same way it is possible to select the odd display rows Di first in accordance with Fig. 4C and next in accordance with Fig 4D.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The embodiments describe an ALIS PDP with plasma channels extending in the horizontal direction. Alternatively, the PDP may be rotated over 90° such that the plasma channels extend in the vertical direction. The plasma channels may be open towards each other such that a layer of plasma exists. Instead of plasma channels, the PDP may comprise plasma cells.
To conclude, an aspect of the invention is defined in a method of displaying a video signal Vs with m video lines in a video field period on a plasma display panel 1 having n display lines Di. The n display lines Di are selected 2 in an interlaced way to subsequently select a first and a second field of n/2 display lines Di to display an interlaced video signal Vs. For displaying a progressive video signal Vs, the m video lines are alternately displayed 3 on the first field of display lines Di only, or on the second field of display lines Di only, both during respective time periods which are longer than the video field period.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of other elements or steps than those listed in a claim. The invention can be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware.

CLAIMS:

1. A method of displaying a video signal (Vs) with video lines in a video field period on a plasma display panel (1) having a first and a second display field of display lines, the display lines (Di) of the first display field being positioned interlaced with respect to the display lines (Di) of the second display field, the method comprising the steps of:

alternately selecting (2) several times the first display field only, or the second display field only, both during respective time periods being longer than the video field period, and

supplying (3) video data signals (Dsj) in conformance with the video lines to the display lines (Di) of the selected display field.

2. A method as claimed in claim 1, characterized in that a number of video lines in a video field period is smaller than or substantially equal to the number of display lines (Di) of the first or second display field.

3. A method as claimed in claim 1, characterized in that the time periods are substantially longer than the video field period.

4. A circuit for displaying a video signal (Vs) with video lines in a video field period on a plasma display panel (1) having a first and a second display field of display lines, the display lines (Di) of the first display field being positioned interlaced with respect to the display lines (Di) of the second display field, the circuit comprising:

means (2) for alternately selecting several times the first display field only, or the second display field only, both during respective time periods being longer than the video field period, and

means (3) for supplying video data signals (Dsj) in conformance with the video lines to the display lines (Di) of the selected display field.

5. A plasma display device comprising a plasma display panel (1) and a circuit for displaying a video signal (Vs) with video lines in a video field period on a plasma display panel (1) having a first and a second display field of display lines, the display lines (Di) of the first display field being positioned interlaced with respect to the display lines (Di) of the second display field, the circuit comprising:

means (2) for alternately selecting several times the first display field only, or the second display field only, both during respective time periods being longer than the video field period, and

means (3) for supplying video data signals (Dsj) in conformance with the video lines to display lines (Di) of the selected display field.

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ABSTRACT:

In a method of displaying a video signal (Vs) with m video lines in a video field period on a plasma display panel (1) which has n display lines (Di). The n display lines (Di) are selected (2) in an interlaced way to subsequently select a first and a second field of n/2 display lines (Di) to display an interlaced video signal (Vs). For displaying a progressive video signal (Vs), the m video lines are alternately displayed (3) on the first field of display lines (Di) only, or on the second field of display lines (Di) only, both during respective time periods which are longer than the video field period.

(Fig. 3)

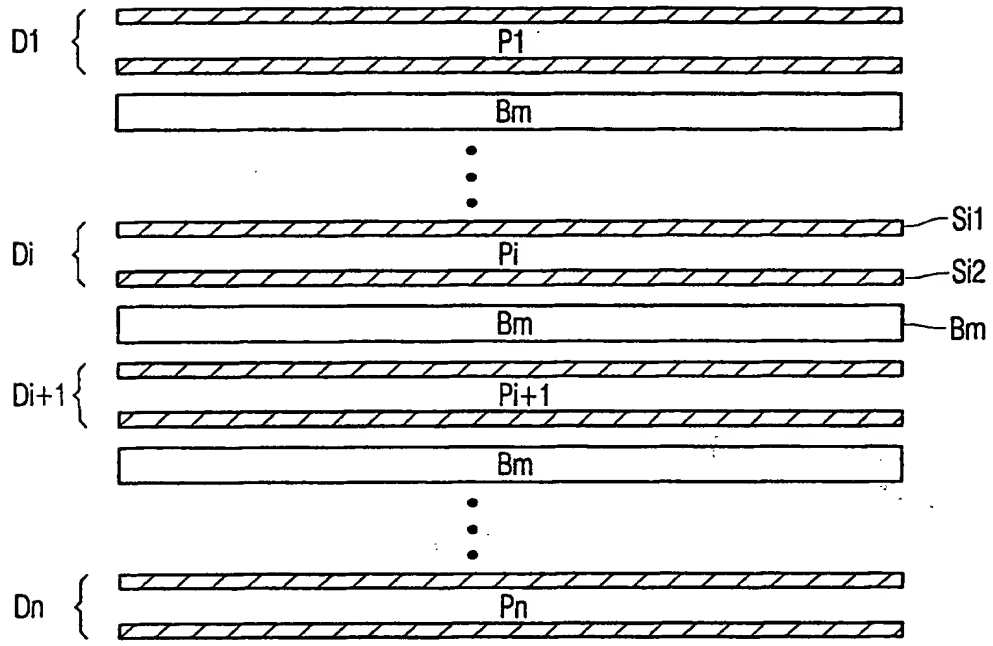


FIG. 1

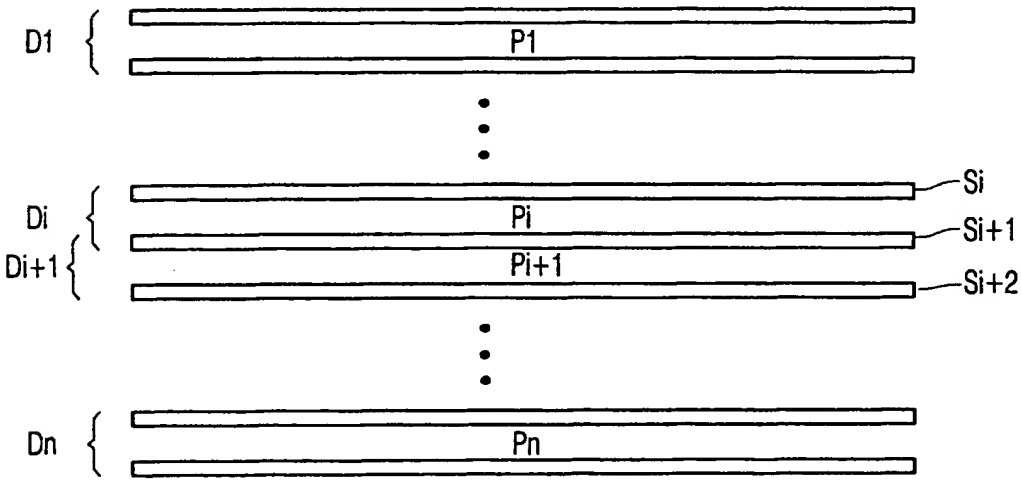


FIG. 2

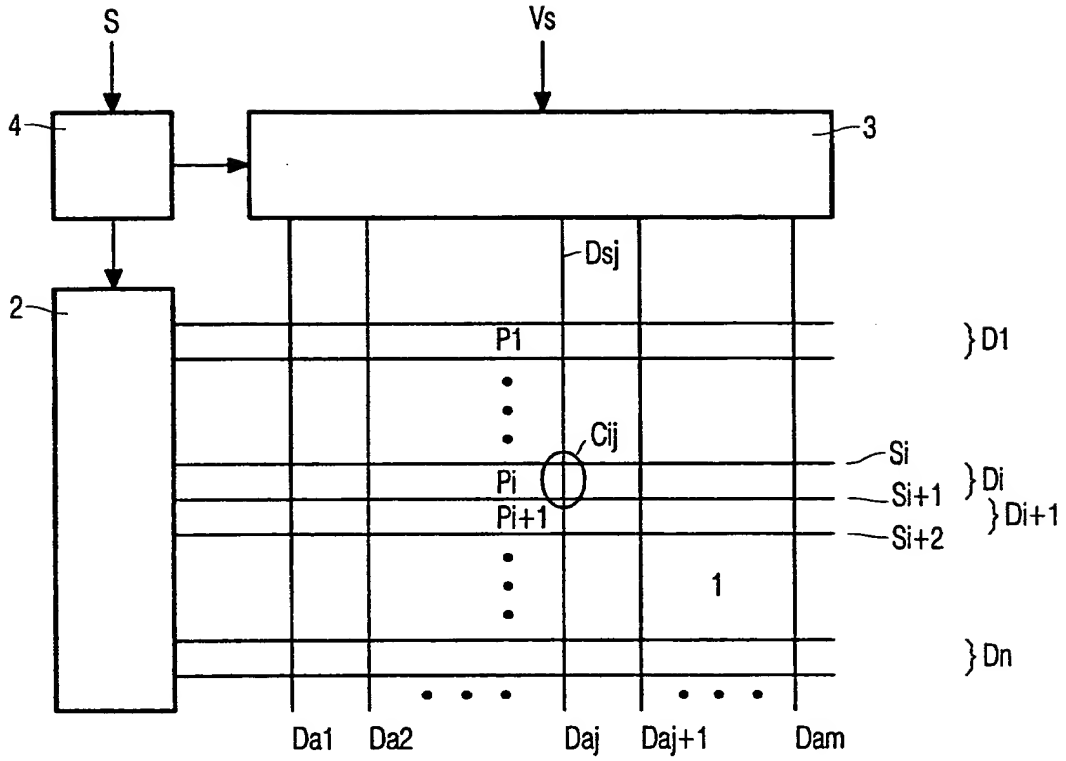
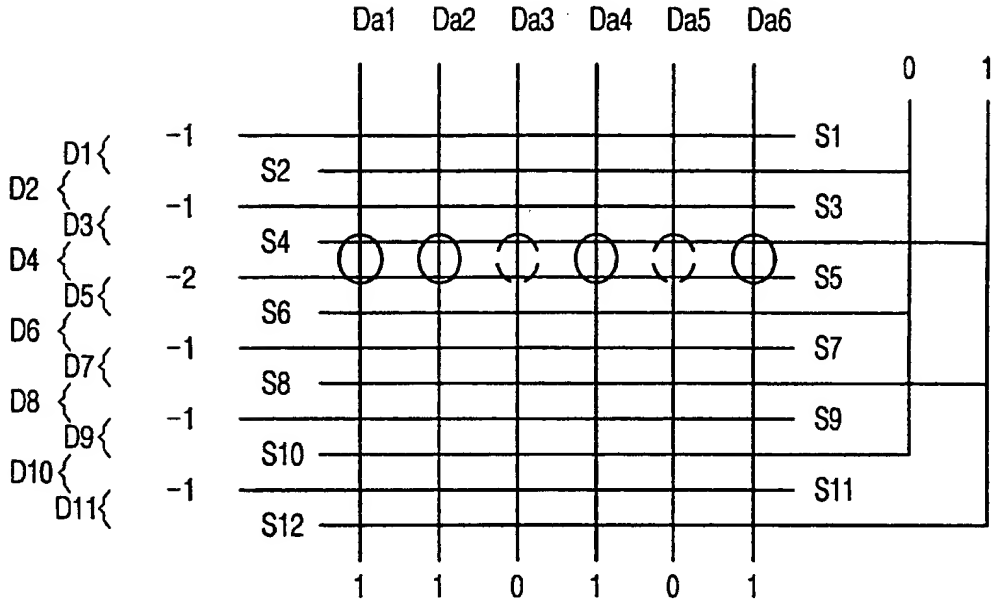

S
Vs
4
3
2
Dsj
P1
Cij
Pi
Pi+1
1
Si
Si+1
Si+2
D1
Di
Di+1
Dn
Da1
Da2
Daj
Daj+1
Dam

FIG. 3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Da2
Da3
Da4
Da5
Da6
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1
D1
D2
D3
D4
D5
D6
D7
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D9
D10
D11
-1
-1
-2
-1
-1
-1
S1
S2
S3
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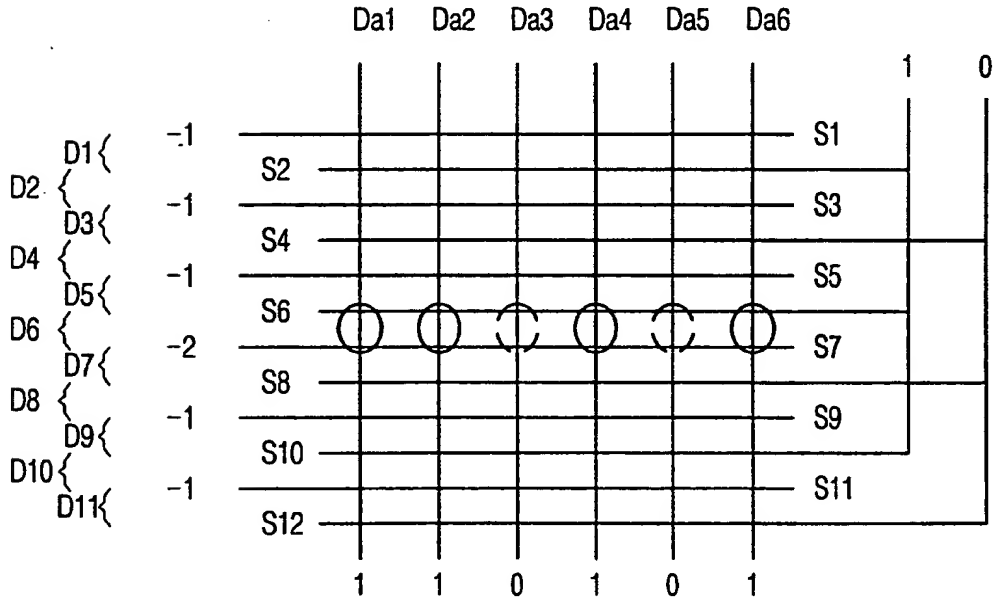
S8
S9
S10
S11
S12
1
1
0
1
0
1

FIG. 4A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-1
S1
S2
S3
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S12
1
1
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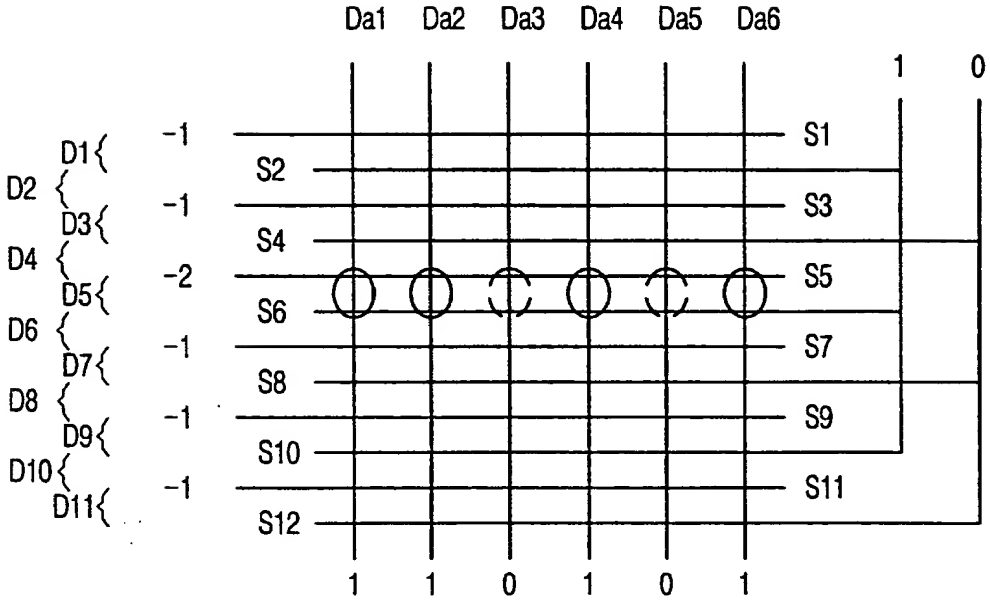
0
1

FIG. 4B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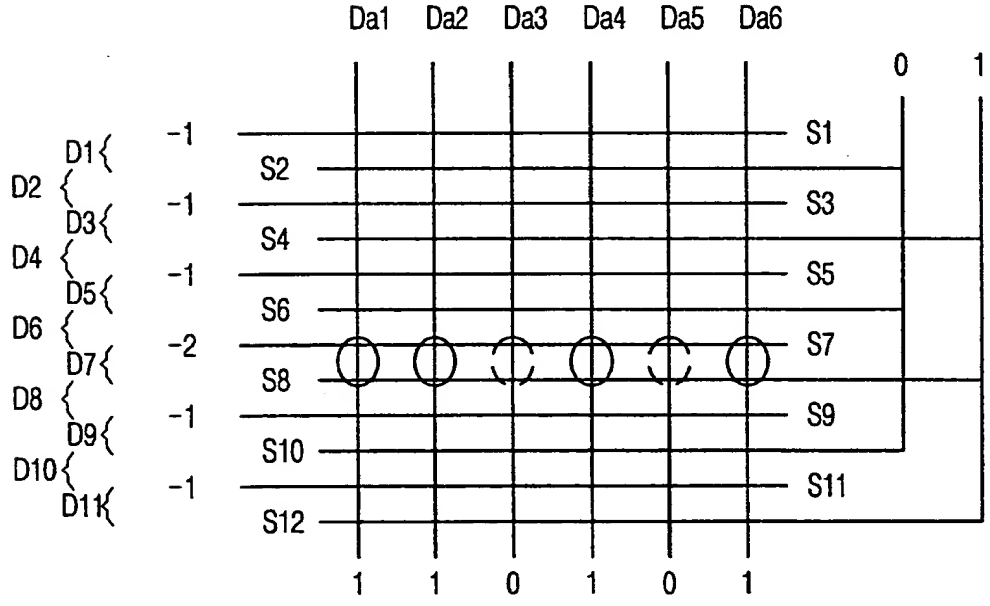
1 0
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11
-1 -1 -2 -1 -1 -1
S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12
1 1 0 1 0 1

FIG. 4C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D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11
-1 -1 -1 -2 -1 -1
S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12
1 1 0 1 0 1

FIG. 4D